REMARKS

The amendment to claims 1 and 18 incorporates the limitation of original claim 8 and the time limitation specified three lines from the end of paragraph 0045 of the specification. The amendment to claim 11 is supported by original claim 1. is merely the incorporation of original claim 6 into original 1. New claim 20 is supported by the disclosure at paragraph 0045, line 7 (midway through the paragraph). Applicants submit that the amendment does not add any new matter to the disclosure.

Applicants submit that the cancelation of claims 6 and 8 and the proper indication of temperature in amended claims 1 and 18 addresses the rejection of original claims 6 and 8 under 35 USC 112, second paragraph. Applicants submit that the amendment to claim 11 addresses the lack of antecedent basis and places claim 11 in compliance with 34 USC 112, second paragraph.

The invention centers on methods of forming sub-50nm pitch features using lithgraphy. The invention is characterized by the use of resist having low activation energy acid labile protecting groups and by the use of a controlled low temperature post-exposure treatment. This combination allows for the creation of such fine features while avoiding blur.

Varanasi et al. (US 2003/0182534 A1) discloses a process using photoresist which may contain low activation energy protecting groups. Varanasi et al. uses a conventional post-exposure bake step of involving treatment at 100°C or greater. While Varanasi et al. references a feature size of 130nm or less, the smallest feature size actually resolved in Varanasi et al. is on the order of 150nm. Varanasi et al. does not disclose or suggest the claimed combination of using a photoresist of low activation energy and mild post-exposure treatment,

PAGE 8/9 * RCVD AT 1/18/2005 11:19:24 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):02-18

nor the results associated with such combination, namely the ability to resolve features at 50 nm half pitch.

Yamada et al. (US 6,399,273) discloses specifid photoresists which are thermally treated prior to exposure where the photoresists have improved etch resistance. Yamada discloses a lithography process using a post-exposure bake condition of at least about 60°C, more preferably at least about 100°C. The temperatures actually used in the examples of Yamada et al. are at least 120°C. The features resolved in the examples of Yamada et al. are on the order of 1000 nm. Applicants submit that the combination of Yamada et al. with Varanasi et al. would still result in the use of a post-exposure treatment at temperatures exceeding the claimed range. The combination of Yamada et al. with Varanasi et al. would still fail to disclose or suggest the claimed combination of using a photoresist of low activation energy and mild post-exposure treatment, nor the results associated with such combination, namely the ability to resolve features at 50nm half pitch.

For the above reasons, applicants submit that the claims are patentable and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
David R. Medeiros et al.

By _____
Steven Capella, Attorney
Reg. No. 33,086
Telephone: 845-894-3669

PAGE 9/9 * RCVD AT 1/18/2005 11:19:24 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):02-18 E.09 **